NEC

Customer Notification

V850ES/SG3, V850ES/SJ3

32-bit Single-Chip Microcontrollers

Operating Precautions

**μPD70F3333, μPD70F3334, μPD70F3335,
μPD70F3336, μPD70F3340, μPD70F3341,
μPD70F3342, μPD70F3343, μPD70F3344,
μPD70F3345, μPD70F3346, μPD70F3347,
μPD70F3348, μPD70F3350, μPD70F3351,
μPD70F3352, μPD70F3353, μPD70F3354,
μPD70F3355, μPD70F3356, μPD70F3357,
μPD70F3358, μPD70F3364, μPD70F3365,
μPD70F3366, μPD70F3367, μPD70F3368**

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(A) Table of Operating Precautions

No.	Outline		μPD70F3333, μPD70F3335	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable
✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F3334, μPD70F3336	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD70F3340, µPD70F3350	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F3341, μPD70F3351	
		Rev.	1.0	
		Rank[Note]	I	
1	Setting of DTFR register (Specification change notice)		✗	
2	TMP and TMQ Capture Operation (Specification change notice)		✗	
3	Flash security flag setting (Technical limitation)		✓	
4	Boot swap function of selfprogramming (Technical limitation)		✓	
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD70F3342, µPD70F3352	
		Rev.	1.0	
		Rank[Note]	I	
1	Setting of DTFR register (Specification change notice)		✗	
2	TMP and TMQ Capture Operation (Specification change notice)		✗	
3	Flash security flag setting (Technical limitation)		✓	
4	Boot swap function of selfprogramming (Technical limitation)		✓	
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F3343, μPD70F3353	
		Rev.	1.0	
		Rank[Note]	I	
1	Setting of DTFR register (Specification change notice)		✗	
2	TMP and TMQ Capture Operation (Specification change notice)		✗	
3	Flash security flag setting (Technical limitation)		✓	
4	Boot swap function of selfprogramming (Technical limitation)		✓	
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD70F3344, µPD70F3354, µPD70F3364	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F3345, μPD70F3355, μPD70F3365	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD70F3346, µPD70F3356, µPD70F3366	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD70F3347, μPD70F3357, μPD70F3367	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD70F3348, µPD70F3358, µPD70F3368	
		Rev.	1.0	1.1
		Rank[Note]	I	I
1	Setting of DTFR register (Specification change notice)		✗	✗
2	TMP and TMQ Capture Operation (Specification change notice)		✗	✗
3	Flash security flag setting (Technical limitation)		✗	✓
4	Boot swap function of selfprogramming (Technical limitation)		✗	✓
5	AFCAN: Sleep Mode Wakeup (Specification change notice)		✗	✗

✓: Not applicable

✗: Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	Setting of DTFR register (Specification change notice)

Details

When the DTFR register is written a DMA request may occur.
When rewriting the IFCn5...IFCn0 flags of the DTFR register, the following bit may be set:
a) DFn bit of the same register in which IFCn5...IFCn0 are set.
b) DFm bit of a DMA channel with a lower priority than that of the DMA channel for which IFCn5...IFCn0 are set but only if IFCn5...IFCn0 are equal to IFCm5...IFCm0.

Workaround

1.) Stop the DMA transmission of DMA channels that apply to the above description.
2.) Check if the DFn(m) bit corresponding to the above description is “0” after rewriting IFCn5...IFCn0.

No. 2	TMP and TMQ Capture Operation (Specification change notice)

Details

When the input capture function is selected for Timer P or Timer Q and a clock of fxx/8 or slower is selected as the count clock for this timer the following applies:
When a capture signal is input during the first count clock after TPnCE=1 for Timer P (TQnCE=1 for Timer Q resprectively) the capture operation is not executed and the corresponding capture interrupt is not issued.

Workaround

There is no workaround.

No. 3	Flash security flag setting (Technical limitation)

Details

It may not be possible to use or clear the security flag of the flash memory.

Workaround

There is no workaround. Do not use the security flag setting function in the flash programmer.

No. 4	Boot swap function of selfprogramming (Technical limitation)
	Details It may not be possible to use the boot swap function in selfprogramming mode. *Workaround* There is no workaround. Do not use the boot swap function.

No. 5	AFCAN: Sleep Mode Wakeup (Specification change notice)

Details:

1. Exclusions

This Operating Precaution is ***only applicable*** to applications, which are fulfilling at least one of the following three conditions:

- SLEEP Mode of AFCAN is used ***and*** the possibility to wake up AFCAN by CAN-Bus events is given (see Remarks: 1.)
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see Remarks: 2.) ***and***
  - after waking up from SLEEP mode of the AFCAN macro, the application software does ***not*** wait until the SLEEP mode is released by polling the CnCTRL (PSMODE) register, before continuing operation with the AFCAN macro (see Remarks: 3.) ***and***
  - the CPU can reach instructions, where AFCAN registers are accessed while the AFCAN macro is still in SLEEP mode, due to the missing waiting condition.
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see Remarks: 2.) ***and***
  - after waking up from SLEEP mode of the AFCAN macro, the CAN Bus Transceiver generates a ***long-lasting or permanent dominant level*** to the CRXD input of the AFCAN macro, instead of the propagated CAN-Bus level.

Remarks: 1. If the CAN-Bus Transceiver does not propagate the CAN-Bus signal, while the AFCAN macro is in SLEEP mode, and also does not forward a wakeup signal to CRXD, ***this Operating Precaution is not applicable.***

2. The clock supply to the AFCAN macro can be stopped, depending on the features of the device, and the system design of the application. If the clock supply to the AFCAN macro is stopped, while a wakeup condition occurs, ***this Operating Precaution is not applicable***.

3. The maximum waiting time for this loop can be up to 10 bits of the CAN-Bus Baudrate.
Waiting while retrying to clear CnINTS (Bit 5) can be used alternatively.

All other applications are not affected by this Operating Precaution.

2. Description

When the AFCAN macro is set into SLEEP mode, it can be woken up by CAN bus activity.

This waking up is asynchronous to the operation of the macro and the CPU. By configuration setting, a WAKEUP interrupt can be generated by the AFCAN macro on the wakeup event.

While the interrupt is generated asynchronously, the AFCAN macro may need another dominant edge on the CAN bus, or software clearing of the SLEEP mode, in order to restart its synchronous operation.

During the time, after the interrupt already has been indicated, and before the CAN macro has restarted its synchronous operation, the registers of the AFCAN macro will not operate, because the AFCAN macro still remains in SLEEP mode. This time we will refer to as “wakeup dead time” in the following context.

No. 5	AFCAN: Sleep Mode Wakeup (Specification change notice)

To resolve from the wakeup dead time, software and/or hardware measures are required.

Note: However, this Precaution does *not apply to all* applications. Only dedicated applications are affected (see above).

3. Application Dependency

3.1 Overview

The following flowchart illustrates, how and whether additional measures have to be taken in software, to avoid the *wakeup dead time*.

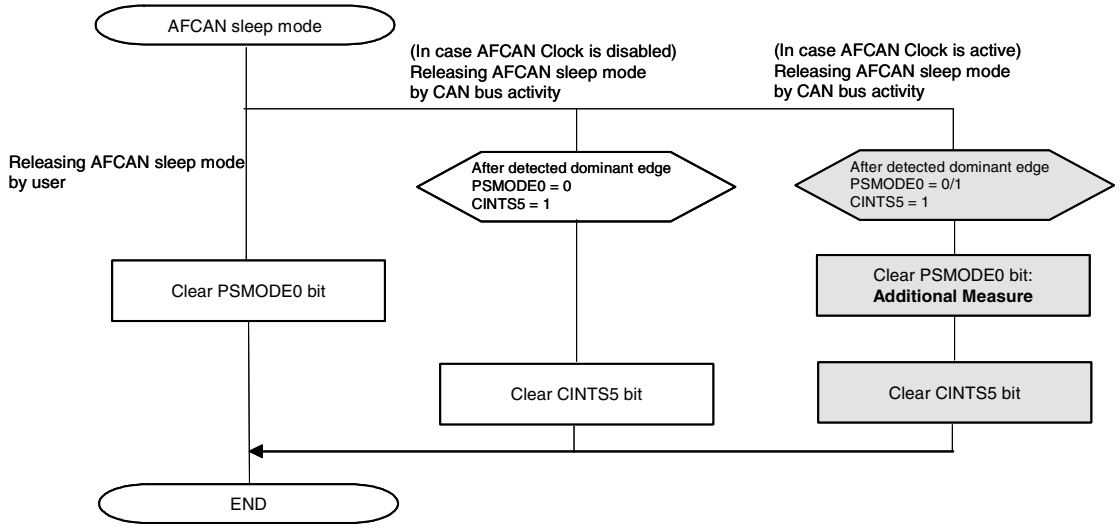

Figure 3-1: Additional Measures in case AFCAN clock is active when waking up

3.2 Not affected Applications

3.2.1 Applications not using SLEEP mode

If SLEEP mode is not used, ***this Operating Precaution is not applicable.***

3.2.2 Applications waking up from SLEEP mode by User Request only

If there is no condition, when SLEEP mode can be left by CAN-Bus activity, but only on User Request (by clearing the PSMODE flag by software), ***this Operating Precaution is not applicable.***

No. 5	AFCAN: Sleep Mode Wakeup (Specification change notice)

3.2.3 Applications using a CPU Power Save Mode

If the clock to the AFCAN macro is disabled, while it is woken up from SLEEP mode, ***this Operating Precaution is not applicable.***

This means, if the user selects a power save mode of the target device, which switches off the clock of the AFCAN macro, immediately after it had been set into SLEEP mode, like the *"CPU STOP"* mode, the precaution needs not to be considered.

This is associated with the software improvement hints below.

3.3 Affected Applications

3.3.1 Applications not waiting until SLEEP mode is left

If Bus Transceivers are used in conjunction with AFCAN, which will *propagate the CAN-Bus signal* to AFCAN permanently (not switched off or not in power saving modes), or, if Bus Transceivers are used in conjunction with AFCAN, which will *propagate the unmodified CAN-Bus signal* when waking up from a power save mode, the *wakeup dead time* lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal.

The worst case (maximum length) of the *wakeup dead time*, is given by the CAN bus speed and the rule of the CAN bus about the frequency of recessive-to-dominant edges. Given by the stuffing rule, at least every 10 bits, a recessive-to-dominant edge must occur.

If during the *wakeup dead time,* the CPU waits until the SLEEP mode is indicated to be cleared (either by polling the PSMODE flag, or by retrying to clear CnINTS[5]), ***this Operating Precaution is not applicable. In this case, the Improvement Hint according to 4.2.2 is followed implicitly.***

If during the *wakeup dead time,* the CPU does not perform any access to the AFCAN macro in any case, ***this Operating Precaution is not applicable.***

3.3.2 Applications using Bus Transceivers generating long-lasting dominant CAN-Bus Signals

If Bus Transceivers are used in conjunction with AFCAN, which *generate a permanent or long-lasting dominant level* when waking up from a power save mode, the Operating Precaution must be considered in any case.

In this case, the *wakeup dead time* lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal, depending on the behaviour of the CAN-Bus Transceiver.

If no further dominant edge on the CAN bus occurs (in case of some CAN Transceivers, which only provide one single edge on waking up), the time until SLEEP mode is left may become endless. Therefore, the waking up procedure of AFCAN regarding software, must be adjusted according to 4.1.1.

No. 5	AFCAN: Sleep Mode Wakeup (Specification change notice)

4. Software Improvement Hints

4.1 Recommended WAKEUP Handling by Software

4.1.1 Clearing the SLEEP Mode by Software

Within the WAKEUP interrupt routine, before accessing any other register or area of AFCAN, the SLEEP mode can be canceled by software, followed by a clearance of the WAKEUP interrupt flag.

Doing so, the AFCAN macro will start its synchronous operation right after these accesses.

In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

```
WAKEUP INTERRUPT VECTOR -->
                          <CnCTRL_PSMODE> = 0;   /* Clear SLEEP Mode */
                          <CnINTS_CINTS5> = 1;   /* Clear INTS5      */
                          ...
                        /* following other parts of interrupt routine */
                          ...
```

Note: Clearing INTS5 is required to get another WAKEUP interrupt anyway, by specification.

4.2 Other WAKEUP Handling Hints

4.2.1 Switching off the Clock Supply to AFCAN, while in SLEEP Mode

If the clock supply to the AFCAN macro is stopped, while it is in SLEEP mode, the synchronisation of the WAKEUP works without any restriction. To achieve this, the documentation of clock controlling unit of the target device should be consulted. Usually this is performed by setting the STOP mode of the CPU of the target device.

However, the user has to consider, that there must not be any WAKEUP condition (dominant level on the CAN-Bus), while the software is executing between setting SLEEP mode and stopping the AFCAN clock.

4.2.2 Using a Waiting Loop within the WAKEUP interrupt routine

Within the WAKEUP interrupt routine, create a waiting loop, which tests the capability of clearing the WAKEUP interrupt flag within AFCAN, by checking the actual power save mode.

In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

No. 5	AFCAN: Sleep Mode Wakeup (Specification change notice)

```
do
{
    AFCAN_SleepStatus = <CnCTRL_PSMODE>

    if( AFCAN_SleepStatus != 0 )
    {
        /* macro is still in SLEEP mode (waiting for latency time) */

        <CnINTS_CINTS5> = 1;    /* repeated trying to clear CINTS5 */
    }

} while( AFCAN_SleepStatus != 0 );
```

This improvement hint *cannot be applied*, if a CAN-Bus-Transceiver is attached to AFCAN, which generates a *permanent or long-lasting dominant level to the CRXD* AFCAN receive input, if a wakeup condition occurs. Missing another dominant edge on the bus, the synchronisation will not happen, and the loop could run endlessly.

4.2.3 Using INIT Mode instead of SLEEP Mode

In this case, the waking up by CAN-Bus activity must be performed via another free Pin I/O Interrupt. Probably, the RX signal of CAN must be distributed on the CRXD of the AFCAN macro, and another Pin I/O in parallel.

Using this Pin I/O Interrupt, the AFCAN macro can be put back into the previous Operation mode.

This implementation will *not* use the SLEEP mode of AFCAN at all, and use the INIT mode instead.

(C) Valid Specification

Item	Date pulished	Document No.	Document Title
1	December 2006	U17790EJ2V0UD00	V850ES/SJ3 Hardware (User's Manual)
2	December 2006	U17728EJ2V0UD00	V850ES/SG3 Hardware (User's Manual)
3	April 2004	U15943EJ3V0UM00	V850ES Architecture (User's Manual)

(D) Revision History

Item	Date pulished	Document No.	Comment
1	Apr. 26, 2006	TPS-HE-B-2580	First release.
2	Jul. 14, 2006	TPS-HE-B-2581	Added item 4, added uPD70F3368.
3	Sep. 2006	TPS-HE-B-2582	Added item 5, added new device versions, added version 1.1 for all actual devices, modified descriptions 3 and 4.
4	Oct. 2006	U18391EE1V0IF00	Added table for 1M devices, new document number format
5	Mar. 2007	U18391EE2V0IF00	Added devices uPD70F3341, uPD70F3342, uPD70F3343, uPD70F3351, uPD70F3352, uPD70F3353.